	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	58793	(rc or (resistance with capacitance))	USPAT	2002/01/16 09:05
2	BRS	L2	23	1 with netlist	USPAT	2002/01/16 09:50
3	BRS	L3	1652	estimat$3 with (signal or wir$3 or path or net) with block$2	USPAT	2002/01/16 09:53
4	BRS	L4	2	3 same (model and (rc or resistance and capacitance))	USPAT	2002/01/16 10:16

DOCUMENT-IDENTIFIER: US 6128768 A
TITLE: Method of extracting layout parasitics for nets of an integrated circuit
using a connectivity-based approach

BSPR:
A user who desires only to extract data on a particular net, such as clock net,
must extract an entire integrated circuit to get the desired information. After this information is obtained and analysis is performed on the net, the
user will want to make changes if the targeted performance goal is not achieved. After any changes are made, a user will need to extract the entire
design once again to perform the required analysis. These design iterations
can take weeks to complete. Even if this method is successfully used, the user
cannot generate a complete distributed RC netlist (which provide greater
accuracy) suitable for timing or interconnect simulation.

BSPR:
The direct simulation method has been implemented to extract small-area layout
parasitics. It is based on user specifying extraction for an area or region of
an integrated circuit. This area is then divided into smaller areas which a
field solver can simulate. However, a drawback is that the field solver takes
a long time to simulate even small areas. Consequently, this approach is
limited to small-area parasitic extraction. Although some improvements to

field solvers have been made, extraction time is still excessive. Furthermore,
a field solver approach cannot generate a complete net-by-net distributed RC
netlist including transistor parameter timing or power simulation.

DEPR:
From Connectivity-Based Database 143, Netlister 147 will generate a netlist
format file of the extracted parasitic resistance and capacitance values.
These extracted parasitic values may be back annotated into the circuit
schematic for circuit simulation. Also, other applications software may use
the netlist format file to produce other integrated circuit analyses including
clock skew analysis, power distribution analysis, timing analysis,
electromigration analysis, coupling analysis, power ground bounce analysis, and
inductance analysis.

DOCUMENT-IDENTIFIER: US 6182269 B1
TITLE: Method and device for fast and accurate parasitic extraction

DEPR:
Referring now to FIG. 1A, showing a flow chart of a preferred embodiment of the invention, the process begins at block 100, which may be initiated by another program or module. Block 102 selects a net and determines a port-to-port net length and a total net length from layout database 104. The port-to-port net length, that is, the net length from the output port of the driver cell to the input port of the load cell, is required to evaluate net resistance. Block 106 determines the estimated net resistance (R.sub.net) of the net by multiplying the port-to-port net length with a resistance per unit length value (R.sub.per unit length) obtained from technology file 108. The R.sub.per unit length may be a constant value to simplify the estimation calculation. Furthermore, the R.sub.per unit length value may be associated with the net or with a subset of nets based on known characteristics, such as the number of vias or metals layers.

DEPR:
Likewise, block 106 also determines an estimated net capacitance (C.sub.net) of the net by multiplying the total net length with a capacitance per unit length

value (C.sub.per unit length) obtained from technology file 108. The total net
length, that is, the sum of the net lengths from the output port of the driver
cell to all fanout branches on the net, is required to evaluate net capacitance. The C.sub.per unit length may also be a constant value to
simplify the estimation calculation. Furthermore, the C.sub.per unit length
value may be associated with the net or with a subset of nets based on known
characteristics, such as the number of vias or metals layers.

DEPR:
Block 126 performs a detailed impedance extraction on each net in the list of
"critical nets." The detailed impedance extraction employs a distributed
impedance model. In a preferred embodiment, the STAR-R tool from AVANT!
CORPORATION, employing a distributed impedance model, performs this function.
In block 128, the detailed parasitic impedance values of critical nets are
merged with the estimated net impedance values of noncritical nets (R.sub.net
and C.sub.net). The merged impedance data is then available for input into
subsequent calculation steps, which may be executed after block 130.

DOCUMENT-IDENTIFIER: US 6286126 B1
TITLE: Methods, apparatus and computer program products for performing post-layout verification of microelectronic circuits using best and worst case delay models for nets therein

BSPR:
Attempts have also been made to reduce the complexity of extraction by applying heuristic approaches, such as by selecting only clock nets, "top level" nets, nets with large total capacitance or nets within preselected timing critical paths determined by simplified simulation techniques. For example, traditional attempts to account for the timing delays associated with interconnect nets typically include the steps of performing detailed extraction only after timing critical paths have already been determined. As illustrated best by FIG. 2, such attempts include the steps of supplementing a circuit netlist with unbounded parasitic estimates of the resistance and capacitance of the interconnect nets and then performing a timing simulation of the circuit to identify potential timing critical paths. Detailed parasitic extraction of those nets in the timing critical paths may then be performed to determine an updated estimate of the delay associated with the timing critical paths.
Unfortunately, these and related attempts typically rely on relatively inaccurate parasitic estimates based on simplified models which can cause the

timing analysis tool to select "false" critical paths and miss "real" critical
paths. This means that necessary detailed parasitic extraction may not be
performed on some layout critical nets.

DOCUMENT-IDENTIFIER: US 5974247 A
TITLE: Apparatus and method of LSI timing degradation simulation

DEPR:
The LSI netlist 9 is described in a format such as a DSPF (Detailed Standard Parasitic File), which is written in Cadence Standard Parasitic Format (1993) pp.8-20 by Cadence Design Systems, Inc. To achieve higher accuracy, it is preferable that the LSI netlist 9 includes parasitic element information such as the parasitic capacitance or parasitic resistance of a wire between circuit cells. The delay library 13 uses the output load capacitance and the rise and fall times of the input signal of a circuit cell as predetermined operational conditions. In short, in the delay library 13 the dependence of the delay of each circuit cell on the operational conditions when the LSI has not been degraded is stored.

DEPR:
In the present embodiment the before-degradation LSI timing 8 and the after-degradation LSI timing 14 include a delay of a circuit cell only; however, they may also include the wiring delay between circuit cells. In this case, the delay calculator 12 is supposed to read parasitic element information such as wiring resistance or wiring capacitance from the LSI netlist 9, further read the driving property (such as output impedance or output current) of the

output terminals from the delay library 13, calculate the delay of the wire
which is connected to the output terminals of the circuit cells based on the
read information and driving property, and output the calculated results to the
before-degradation LSI timing 8 and the after-degradation LSI timing 14. Thus,
more accurate logic simulation can be achieved.

DOCUMENT-IDENTIFIER: US 5901063 A
TITLE: System and method for extracting parasitic impedance from an integrated circuit layout

DEPR:
For each net analyzed, RC network module 404 combines the RC networks of all the change areas of the net to provide a full RC netlist model for the net. RC network module 404 includes an RC network reduction module 405, which can be used to reduce the full RC netlist model to provide a reduced RC netlist model, using well-known linear network reduction techniques. The reduced RC netlist model is suitable for obtaining better runtime performance in some delay calculators.

DOCUMENT-IDENTIFIER: US 5896300 A

TITLE: Methods, apparatus and computer program products for performing post-layout verification of microelectronic circuits by filtering timing error bounds for layout critical nets

BSPR:

Attempts have also been made to reduce the complexity of extraction by applying heuristic approaches, such as by selecting only clock nets, "top level" nets, nets with large total capacitance or nets within preselected timing critical paths determined by simplified simulation techniques. For example, traditional attempts to account for the timing delays associated with interconnect nets typically include the steps of performing detailed extraction only after timing critical paths have already been determined. As illustrated best by FIG. 2, such attempts include the steps of supplementing a circuit netlist with unbounded parasitic estimates of the resistance and capacitance of the interconnect nets and then performing a timing simulation of the circuit to identify potential timing critical paths. Detailed parasitic extraction of those nets in the timing critical paths may then be performed to determine an updated estimate of the delay associated with the timing critical paths.

Unfortunately, these and related attempts typically rely on relatively inaccurate parasitic estimates based on simplified models which can cause the

timing analysis tool to select "false" critical paths and miss "real" critical
paths. This means that necessary detailed parasitic extraction may not be
performed on some layout critical nets.

DOCUMENT-IDENTIFIER: US 5629860 A
TITLE: Method for determining timing delays associated with placement and routing of an integrated circuit

DEPR:
Following the step calculate parasitics (25) is the step convert delay equation as represented by circle 29. The inputs to circle 29 are design constraints (2), netlist (3), macrocell groups (5), cell library characteristics (10), net type (26), RC time constant (27) and lumped capacitance (28) and the output is net parasitics (30). The design constraints (2), netlist (3), macrocell groups (5) and cell library characteristics (10) all of which have been aforedescribed. The cell library characteristics (10) additionally define the cell drive strengths. Output net parasitics as represented by box 30 is a list of wire delay estimates sorted by net type (26) and macrocell group (5).

DOCUMENT-IDENTIFIER: US 6189131 B1
TITLE: Method of selecting and synthesizing metal interconnect wires in integrated circuits

DEPR:
After full place and route of the design in step 334, better timing accuracy is available because precise wire lengths can be extracted. As noted above, signal delays are highly correlated with wire resistance and capacitance, some of which is due to wire length, and some of which is due to three-dimensional parasistic capacitive effects resulting from multi-level routing. The full chip layout database may be analyzed to generate a parasitic RC (resistance-capacitance) netlist. Timing delays may then be computed, and the results fed back to synthesis tools and floorplanning tools for timing verification.